

**Notic of References Cited**

Application/Control No.

08/807,737

Applicant(s)/Patent Under  
Reexamination  
OHTANI ET AL.

Examiner

Evan T. Pert

Art Unit

2813

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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification	
X	A	US-5,643,826-	07-1997	Ohtani et al.	--	--
	B	US- -				
	C	US- -				
	D	US- -				
	E	US- -				
	F	US- -				
	G	US- -				
	H	US- -				
	I	US- -				
	J	US- -				
	K	US- -				
	L	US- -				
	M	US- -				

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification	
	N	JP-6-267978-A	09-1992	Japan	Chiyou et al.	--	--
	O	- -					
	P	- -					
	Q	- -					
	R	- -					
	S	- -					
	T	- -					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Wolf, SILICON PROCESSING FOR THE VLSI ERA VOLUME 2: PROCESS INTEGRATION, 1990, Lattice Press, page 274.
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\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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